

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A TFT array substrate, comprising:

a thin film transistor section in which a gate electrode is formed on a substrate, and in which a semiconductor layer that has been etched after a mask material is dropped onto a semiconductor film is formed on the gate electrode via a gate insulation layer,

the processed formed semiconductor layer having a shape formed by dropping a droplet.

2. (Original) The TFT array substrate as set forth in claim 1, wherein:

the gate electrode in the thin film transistor section is a branch electrode which is branched out of a main line of the gate electrode, and the branch electrode has an open end protruded from an area for the semiconductor layer.

3. (Original) The TFT array substrate as set forth in claim 2, wherein:

the branch electrode is arranged so that a portion protruded from the area for the semiconductor layer is smaller in width than a portion confined within the area for the semiconductor layer.

4. (Original) The TFT array substrate as set forth in claim 2, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain

electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed in contact with one of the source and drain electrodes.

5. (Original) The TFT array substrate as set forth in claim 2, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed according to the following formula (1),

$$L3 > r + \Delta 1 + 2\Delta 2 \quad \dots (1)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, $\Delta 2$ denotes a second error taking account of dropping off a target position, and $L3$ denotes a distance from the center of the channel section to the open end of the branch electrode.

6. (Original) The TFT array substrate as set forth in claim 2, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed according to the following formula (2),

$$L2 > \Delta 1 + 2\Delta 2 \quad \dots (2)$$

where $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping,

Δ_2 denotes a second error taking account of dropping off a target position, and L_2 denotes a distance from (1) an end of each of the source and drain electrodes, closer to the open end of the branch electrode, to (2) the open end of the branch electrode.

Claims 7.-8. Cancelled.

9. (Original) The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the semiconductor layer is formed according to the following formula (3),

$$R > r + \Delta_1 + \Delta_2 \dots (3)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, Δ_1 denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, Δ_2 denotes a second error taking account of dropping off a target position, and R denotes a radius of the semiconductor layer, which extends from the center of the channel section.

10. (Original) A liquid crystal display device including the TFT array substrate as set forth in claim 1.

Claims 11.-25. Cancelled.

26. (Currently Amended) A TFT array substrate, comprising:

a thin film transistor section in which a gate electrode is formed on a substrate, and in which a semiconductor layer that has been etched after a mask material is dropped onto a semiconductor film and a conductor layer are formed on the gate electrode via a gate insulation layer,

wherein:

the conductor layer is formed in contact with the semiconductor layer and one of source and drain electrodes of the thin film transistor section, and has a portion formed by dropping a droplet, the conductor layer and the semiconductor layer having substantially the same shape in the portion formed by dropping a droplet.

27. (Original) The manufacturing method of a TFT array substrate as set forth in claim 26, wherein:

the conductor layer is constituted of Mo, W, Ag, Cr, Ta, Ti, a metal material mainly containing one of Mo, W, Ag, Cr, Ta, Ti, or an indium tin oxide.

28. (Original) The manufacturing method of a TFT array substrate as set forth in claim 27, wherein:

the source and drain electrodes are made of an Al or a metal material mainly containing Al.

29. (Original) A liquid crystal display device including the TFT array substrate as set forth in claim 26.

30. (Original) A manufacturing method of a TFT array substrate, comprising the steps of:

- (a) forming a gate electrode on a substrate;
- (b) forming a gate insulation layer on the gate electrode;
- (c) depositing a semiconductor film on the gate insulation layer;
- (d) forming a conductor forming layer having a shape of a droplet by dropping a droplet of a conductive material on the semiconductor film, and
- (e) forming a semiconductor layer of a thin film transistor section by processing the semiconductor film corresponding to the shape of the conductor forming layer.

Claims 31.-33. Cancelled.

34. (Original) An electronic device including the TFT array substrate as set forth in claim 1.

35. (Original) An electronic device including the TFT array substrate as set forth in claim 26.